Synopsys TestMAX

Test all the Limits

Overview

Synopsys TestMAX delivers AI-driven Test as part of the Synopsys.ai hyperconvergent EDA stack that overcomes the silicon design, test, and analytics challenges of advanced technologies.

Industry Test Challenges

- Turn-around Time
- Cost and Quality
- Scalability
- Engineering resources

Key Segment Needs

Automotive

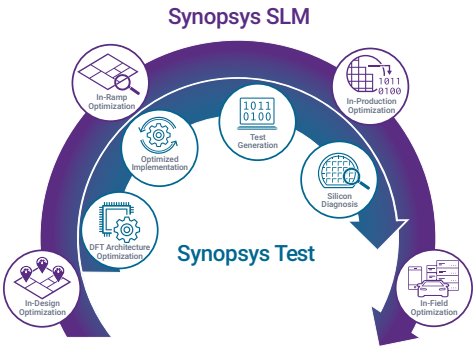
- High Defect Coverage
- Optimal In-system Test Time and Coverage
- Power-on/off & IST controller
- ASIL Quality Requirements

AI/Hyperscaler

- Scalable Test Architecture
- RTL-based Hierarchical Test
- High Identical Core Compression
- Physical Design Flexibility

5G and Consumer

- Advanced Compression
- RTL-based Hierarchical Test
- Maximize Block DFT Reuse
- Fast Runtime & Iterations



SLM & TestMAX Synergy

Synopsys SLM and TestMAX solutions encompass integrated tools, IP and methodologies to test, monitor and analyze SoCs, providing actionable insights at every phase of the system lifecycle.

synopsys.com/test

Synopsys Test Family

Synopsys TestMAX products and technologies are enabled by a common Synopsys TestMAX Manager flow resulting in an industry first RTL to ATE solution. With AI enablement and the connection to synthesis for optimal design, power, performance and area, users can maximize test quality and coverage.

Product		Features	Benefits
Synopsys TestMAX Manager	Scaling and complexity	• Comprehensive RTL editing • Hierarchical pattern porting • Provides a Tcl based framework	• Common interface for all DFT tools • Shift Left enabler • Full RTL flow integration support
Synopsys TestMAX Advisor	Early violation checks	• DFT violation checking • ATPG coverage estimation • Test Points selection	• Fine-tune RTL early in the design • Shorten test implementation time • Minimize congestion and reduce timing impacts
Synopsys TestMAX DFT	Test cost and turnaround time	• High test time and test data reduction • Patented, powerful compression technologies • RTL generation with TestMAX Manager	• Lowers test costs • Enables high defect coverage • Minimizes impact on design power, performance, and area
Synopsys TestMAX ATPG	Test quality, speed and cost	• Automatic test pattern generation for faster runtime • Reduced memory bottlenecks • Consistent results across compute	• Generates high-coverage test patterns more quickly • Lowers test time and cost • Enables highly efficient utilization of hardware resources for ATPG
Synopsys TestMAX XLBIST	Functional safety	• Supports standard and high X-tolerance architectures • Supports deterministic compressed patterns • Intelligent re-seeding and response analysis	• Addresses ISO 26262 automotive functional safety • Predictably achieves target test coverage • X-tolerant logic BIST eliminates designer effort
Synopsys TestMAX ALE	Test coverage shortfalls	• Enables HSIO's with Synopsys HSAT IP for high bandwidth test • Automatically packetizes and depacketizes scan data • Reads in STIL from TestMAX ATPG and generates fail logs	• Minimal pin count interface that accommodates most designs • Easily adapts to support different high-speed input-output interfaces (HSIO) • Simplifies ATE pin electronics for reduced tester costs
Synopsys TestMAX Vtran	Vector translation	• Translates ATPG patterns into various ATE formats • Supports WGL and IEEE 1450 (STIL) conversion • Creates testbenches for Verilog simulation-based verification	• Streamlines production test flow • Reduces turn-around-time by creating validation testbenches • Reduces engineering debug time
Synopsys TestMAX Diagnosis	Defect analysis and time to results	• Quickly finds silicon defect candidates for failure analysis • Supports CAFM (cell-aware) • High throughput with parallel diagnostics of multiple fail logs	• Isolation of systemic defects with volume diagnostics supported by Yield Explorer • Detects FEOL and BEOL defectivity problems • Low TCO diagnosis solution
Synopsys SMS IP	Memory complexity	• Supports Synopsys and 3rd party SRAM/RF/ROM and even CAM, eMRAM and DRAM • High-Performance Core Support • FinFET specific memory test Algorithm programmability	• Complete test, repair, debug and diagnostics • Integrated Test and Repair with Synopsys Embedded Memories • High test coverage minimizing DPPM
Synopsys SHS IP	Multi-die complexity and IP integration	• Automated hierarchical test • Automated test integration of all IP/Cores on SoC • Pre-validated ready ATE patterns with pattern porting	• Accelerate SoC testing • Increase design and DFx productivity • Optimize test time and power
Synopsys TSO.ai	Set up time, scalability & expertise	• Industry-first Test-AI technology • Scales to available compute • Cold / warm start	• Automatically minimizes pattern count for target test coverage • Eliminates random, time-consuming ATPG user-iterations • Removes dependency on tool expertise for optimal ATPG configuration

Support and Services

Synopsys offers expert global support and complete services for all Synopsys TestMAX products and features including Multi-die/IEEE 1838, ISO 26262 compliance and SMS/SHS customizations.

SYNOPSYS®

09/25/23.CS1203392818-TestMAX Flyer.